

Appl. No. : 10/724,534  
Filed : November 26, 2003

### AMENDMENTS TO THE CLAIMS

By this Response, Applicant is amending Claims 1, 4, 12, 31, 33, 40 and is cancelling Claims 21, 32, 34–36, 41 and 49 without prejudice or disclaimer. Claims 2, 3, 5–11, 13–20, 22, 37–39, 42–47 remain as originally filed or previously presented.

1. (Currently Amended) A method of searching a string of data for a match with a test data string, the method comprising:

receiving an instruction to perform a search operation, the instruction comprising a test data string and a starting address for the search operation;

routing the instruction to a data string manipulation circuit capable of performing string manipulation instructions;

routing the starting address for the search operation from the data string manipulation circuit to a cache memory array;

comparing portions of the test data string with consecutive portions of data stored in the cache memory array;

generating a match signal for each portion of the data stored in the cache memory array that matches a respective compared portion of the test data string;

identifying a plurality of match signals indicating the consecutive portions of the data stored in the cache memory array that together match the test data string; and

routing an address of cached data matching the test data string to the data string manipulation circuit.

2. (Original) The method of Claim 1, additionally comprising routing the test data string from the data string manipulation circuit to the cache memory array.

3. (Original) The method of Claim 2, additionally comprising aligning the test data string with the data stored in the cache memory array prior to said act of comparing.

4. (Currently Amended) The method of Claim 1, wherein said acts of identifying a plurality of match signals and routing an address of cached data is performed by a decoder.

5. (Original) The method of Claim 1, wherein the test data string comprises a word.

6. (Original) The method of Claim 1, wherein the test data string comprises a doubleword.

7. (Original) The method of Claim 1, wherein the test data string comprises a quadword.

8. (Original) The method of Claim 1, wherein said act of comparing is performed by a plurality of comparators.

9. (Original) The method of Claim 8, wherein the number of the plurality of comparators is equal to the number of bytes in a cache line of the cache memory array.

10. (Original) The method of Claim 1, wherein said act of comparing is performed with a plurality of subtractors.

11. (Original) The method of Claim 1, wherein said act of comparing is performed in one clock cycle.

12. (Currently Amended) A method of performing a cache search operation within a digital processing system, the method comprising:

receiving an instruction to perform a search operation, the instruction comprising a starting address and a test data string;

routing the instruction to a data string manipulation circuit;

routing the starting address for the search operation from the data string manipulation circuit to a cache memory;

searching a cache line in the cache memory for data that matches the test data string, wherein said cache line comprises more bytes than the test data string;

generating a match signal for each portion of the data stored in the cache memory that matches a respective compared portion of the test data string;

identifying a plurality of match signals indicating sequential portions of the data stored in the cache memory that together match the test data string; and

routing an address of cached data matching the test data string to the data string manipulation circuit.

13. (Original) The method of Claim 12, additionally comprising aligning the test data string with an offset of the starting address prior to said act of searching.

14. (Original) The method of Claim 12, wherein the data string manipulation circuit comprises a bus interface unit.

15. (Original) The method of Claim 12, wherein the data string manipulation circuit comprises a memory controller.

16. (Original) The method of Claim 12, wherein said act of routing an address of cached data is performed by a decoder.

17. (Original) The method of Claim 12, wherein said act of searching the cache line is performed by a plurality of subtractors.

18. (Original) The method of Claim 12, wherein said act of searching the cache line is performed by a plurality of comparators.

19. (Original) The method of Claim 18, wherein the number of comparators is equal to the number of bytes in the cache line.

20. (Original) The method of Claim 12, wherein said act of searching a cache line is performed in a single cycle.

21. (Cancelled)

22. (Original) The method of Claim 12, wherein the test data string comprises a word.

23.-30. (Cancelled)

31. (Currently Amended) A processor comprising:

a data memory comprising a plurality of cache lines, each cache line comprising a plurality of bytes of data;

an instruction processing circuit configured to receive a test data string and an instruction to perform a search operation beginning at a starting address of the data memory, the instruction processing circuit further comprising:

a plurality of inputs coupled to the data memory such that each input is coupled to receive a different one of the plurality of bytes of data of the cache line, and

a plurality of comparators, each comparator coupled to a respective one of the plurality of inputs and configured to compare the byte of data of the cache line received by the respective input with a portion of the test data string, each comparator further configured to generate a match signal when the byte of data matches the compared portion of the test data string, the plurality of comparators

~~the instruction processing circuit~~ further comprising a plurality of outputs; and

a decoder circuit coupled to the plurality of outputs ~~[[of]]~~ to receive match signals from the plurality of comparators ~~instruction processing circuit~~ and configured to identify ~~[[a]]~~ sequential portions of the cache line having data that, when combined, matches ~~at least a portions~~ of the test data string.

32. (Cancelled).

33. (Currently Amended) The processor of Claim 31 ~~[[32]]~~, wherein the number of comparators is equal to the number of bytes in the cache line.

34.-36. (Cancelled).

37. (Original) The processor of Claim 31, wherein the entire cache line is compared to the test data string in one bus cycle.

38. (Original) The processor of Claim 31, wherein the data memory comprises a Level 1 cache.

39. (Original) The processor of Claim 31, wherein the instruction processing circuit further comprises a memory controller.

40. (Currently Amended) A cache memory circuit comprising:

a data source means for holding a data value;

a cache data memory means for holding at least one cache line comprising a plurality of bytes of data; ~~[[and]]~~

means for searching the at least one cache line, wherein said means for searching is coupled to said cache data memory means and said data source means, and wherein said means for searching receives a starting address for a search operation of the at least one cache line and aligns the data value with an

offset of the starting address to search multiple portions of the at least one cache line in one clock cycle for data that matches compared portions of the data value; and

means for detecting a string of matches between the multiple portions of the at least one cache line and the compared portions of the data value.

41. (Cancelled).

42. (Original) The cache memory circuit of Claim 40, wherein the means for searching comprises a plurality of subtractors.

43. (Original) The cache memory circuit of Claim 40, wherein the means for searching comprises a plurality of comparators.

44. (Original) The cache memory circuit of Claim 43, wherein the number of comparators is equal to the number of bytes in the cache line.

45. (Original) The cache memory circuit of Claim 40, wherein the data source means comprises an external string execution circuit.

46 (Original) The cache memory circuit of Claim 45, wherein the external string execution circuit comprises a bus interface unit.

47. (Original) The cache memory circuit of Claim 45, wherein the external string execution circuit is associated with an off-chip memory controller.

48. (Cancelled).

49. (Cancelled).